

	Application No.	Applicant(s)
Notice of Allowability	10/643,970	ARIYOSHI ET AL.
	Examiner	Art Unit
	Trung Dang	2823
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to		
2. The allowed claim(s) is/are <u>1-13</u> .		
3. The drawings filed on are accepted by the Examiner.		
 4.		
 Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 8/20/03 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. ☐ Interview Summary Paper No./Mail Da 08), 7. ☑ Examiner's Amendr	te

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Stephen G. Adrian on 09/17/04.

IN THE CLAIMS

Claim 1, line 22, change "second" to --first--; line 24, change "a" to --an--.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance:

Independent claim 1 and its dependent claims are allowed over the prior art of record because the prior art does not teach or suggest the claimed semiconductor device, which includes the structure of: an opening formed in a first insulation layer exposing part of a low concentration impurity below; a source/drain layer formed at a position aligned with the opening; a second insulation layer covering the gate electrode and the first insulation layer; and a contact hole formed in a width larger

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than that of the opening at a position aligned with the opening in the first insulation layer, the contact hole reaching the source/drain layer from an upper surface of the second insulation layer via the opening.

Independent claim 7 and its dependent claims are allowed over the prior art of record because the prior art does not teach or suggest the claimed semiconductor device, which includes the structure of: a first insulation layer formed on the low concentration impurity layer and the gate electrode; an opening in the first insulation layer exposing part of the gate electrode; a silicide film on the surface of the gate electrode inside said opening; a second insulation layer covering the gate electrode and the first insulation layer; a contact hole reaching the low concentration layer from an upper surface of the second insulation layer; and a source/drain layer formed in the low concentration impurity layer at a position aligned with the contact hole.

All method claims are allowed because they includes process steps that correspond to every element of the structure of either claim 1 or 7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-

272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang Primary Examiner Art Unit 2823

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09/17/04